

Patent  
029419.0015.UTL1

**MARKED-UP VERSION OF AMENDED CLAIMS**

1. (Amended) A micro-leadframe for mounting at least one integrated circuit, comprising:

a flat base having at least one conductive lead pattern etched on the flat base to provide electrically conductive paths for said at least one integrated circuit; and

a plurality of preload extension tabs arranged about said at least one conductive lead pattern, the preload extension tabs protruding at an angle with respect to the flat base to a predetermined height above the flat base.

3. (Amended) The micro-leadframe of claim 2, wherein said at least one integrated circuit [package] further comprises a semiconductor die within the mold cap.

6. (Amended) A micro-leadframe package, comprising:

a flat base having a conductive lead pattern etched on the flat base;

an integrated circuit connected to the conductive lead pattern of the flat base;

a plurality of preload extension tabs arranged about the conductive lead pattern, the preload extension tabs protruding at an angle with respect to the flat base into the integrated circuit [package] to a predetermined height above the flat base.

9. (Amended) The micro-leadframe package of claim 8, wherein [said at least one] the integrated circuit [package] further comprises a plurality of

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[flipchip] lead finger connections between the semiconductor die and the conductive lead pattern.